Notice of Allowability	Application No.	Applicant(s)	
	09/811,456	ISODA, MASAHITO	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 7/22/04*.

2. ☒ The allowed claim(s) is/are *19-59*.

3. ☒ The drawings filed on *03 July 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *09/479,927* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Sam Huang on 8/10/04.

The application has been amended as follows:

In The Claims

Claim 31, line 9, "a high" has been changed to --the high--.

Claim 31, line 11, "a low" has been changed to --the low--.

Claim 36, line 9, "a high" has been changed to --the high--.

Claim 36, line 11, "a low" has been changed to --the low--.

Reasons For The Above Changes

The above changes were made to correct the indefinite problems in the claims.

REASONS FOR ALLOWANCE

2. The indefinite problems of the claims indicated in the last office action have been overcome based on applicant's amendment filed on 7/22/04.

3. Claims 19-59 are allowed.

Claim 19, as amended, is allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit

including a first inverter and a MOS transistor, and a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal while isolating the other one of the differential amplifier and the second circuit from at least one of the first power supply and the second power supply with the recited connections and operations set forth therein.

Claims 20, 21, 48, and 54-57 are allowed because they depend on claim 19.

Claim 22 is allowed for the same reason as indicate in the last office action, i.e., the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal, wherein the control circuit enables the differential amplifier circuit and disable the second circuit when the first and second input signals have amplitudes smaller than a predetermined voltage.

Claims 23 and 24 are allowed because they depend on claim 22.

Claim 25 is allowed for the same reason as indicated in the last office action, i.e., the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal, wherein the control circuit disables the differential amplifier circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage.

Claims 26 and 27 are allowed because they depend on claim 22.

Claim 28, as amended, is allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including a first inverter and a plurality of MOS transistors, and a control circuit for selectively enabling the differential amplifier circuit and the first and second circuits in accordance with a control signal, wherein the differential amplifier circuit and the first circuit are enabled and the second circuit is disabled when the first and second input signals have amplitudes smaller than a predetermined voltage.

Claims 29-31 and 49-53 are allowed because they depend on claim 28.

Claim 33, as amended, is allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including a first inverter and a plurality of MOS transistors, and a control circuit for selectively enabling the differential amplifier circuit and the first and second circuits in accordance with a control signal, wherein the differential amplifier circuit and the first circuit are disabled and the second circuit is enabled when the first and second input signals have amplitudes greater than a predetermined voltage.

Claims 34-37 are allowed because they depend on claim 33.

Claim 38 is allowed for the same reason as indicated in the last office action, i.e., the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling the differential amplifier circuit and one of the first circuit and the second circuit in accordance with a control signal while isolating the other one of the first circuit and the second circuit from the first power supply or the second power supply.

Claims 39-42, 58 and 59 are allowed because they depend on claim 38.

Claim 43 is allowed for the same reason as indicated in the last office action, i.e., the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling the differential amplifier circuit and the second circuit in accordance with a control signal and disabling the other one of the differential amplifier circuit and the second circuit.

Claim 44 is allowed for the same reason as indicated in the last office action, i.e., the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively isolating one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply while enabling the other one of the differential amplifier circuit and the second circuit.

Claim 45 is allowed for the same reason as indicated in the last office action, i.e., the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal while isolating the other one of the differential amplifier circuit and the second circuit form at least one of the first power supply and the second power supply.

Claim 46 is allowed for the same reason as indicated in the last office action, i.e., the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control

circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal and disabling the other one of the differential amplifier circuit and the second circuit.

Claim 47 is allowed for the same reason as indicated in the last office action, i.e., the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively isolating one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply while enabling the other one of the differential amplifier circuit and the second circuit.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Nguyen